

REMARKS

This is a response to the Office Action dated August 15, 2001. Claims 7-11 and 21-47 are pending in the present application. Reconsideration and allowance of pending claims 7-11 and 21-47 in view of the following remarks are requested.

The Examiner has rejected claims 7, 10 and 11 under 35 USC 102(b) as being anticipated by U.S. patent number 5,874,770 to Saia et al ("Saia"). For the reasons discussed below, Applicant respectfully submits that the present invention, as defined by independent claim 7, is patentably distinguishable over Saia.

The present invention, as defined by independent claim 7, teaches a capacitor comprising a ceramic tantalum nitride dielectric situated between a first capacitor electrode and a second capacitor electrode. As disclosed and taught in the present application, ceramic tantalum nitride is a form of tantalum nitride fabricated in an amorphous ceramic mode. The fabrication of ceramic tantalum nitride, as disclosed in detail in the present application, results in a form of tantalum nitride exhibiting different properties than the well-known form of tantalum nitride fabricated in the metallic mode. For example, in the ceramic mode, tantalum nitride exhibits a high dielectric constant, which allows the present invention to utilize fabricated ceramic tantalum nitride as a dielectric to achieve a capacitor having a relatively high capacitance density. See, for example, page 12, lines 6-11 in the present application.

In contrast, Saia does not teach, disclose, or suggest a capacitor comprising a ceramic tantalum nitride dielectric. Saia specifically discloses a capacitor dielectric layer

including amorphous hydrogenated carbon or tantalum oxide. See, for example, Saia, column 2, lines 65-66. Saia further discloses a list of suitable capacitor dielectric materials, including amorphous hydrogenated carbon, tantalum oxide, aluminum oxide, antimony oxide, bismuth oxide, hafnium oxide, niobium oxide, tungsten oxide, yttrium oxide, and zirconium oxide. See, for example, Saia, column 5, lines 39-48. Thus, Saia does not teach, disclose, or suggest a capacitor dielectric comprising tantalum nitride fabricated in the ceramic amorphous mode, as disclosed and taught in the present application. As such, the present invention, as defined by independent claim 7, is patentably distinguishable over Saia.

The Examiner has further rejected claims 21-47 under 35 USC 103(a) as being unpatentable over U.S. patent number 6,146,959 to DeBoer et al (“DeBoer”) in view of U.S. patent number 5,821,168 to Ajay Jain (“Jain”). For the reasons discussed below, Applicant respectfully submits that the present invention, as defined by independent claims 21 and 34, is patentably distinguishable over DeBoer in view of Jain.

The present invention, as defined by independent claim 21, teaches a capacitor comprising a copper first capacitor electrode, a first barrier layer over the first capacitor electrode, a copper seed layer over the first barrier layer, a dielectric comprising tantalum nitride over the copper seed layer, a second barrier layer over the dielectric, and a copper second capacitor electrode. As disclosed and taught in the present application, tantalum nitride can be fabricated in either a ceramic mode or a metallic mode. Conventional tantalum nitride fabricated in the metallic mode has a low resistivity (see, for example,

page 9, lines 8-11 in the present application), whereas tantalum nitride fabricated in the ceramic mode has a high resistivity. See, for example, page 10, lines 6-11 in the present application. Conventional tantalum nitride fabricated in the metallic mode has been used as a metallic barrier layer in semiconductor chips. However, unlike metallic tantalum nitride, tantalum nitride fabricated in the ceramic mode exhibits a high dielectric constant, as discussed above, and can thus be utilized as a dielectric in a capacitor. Thus, the present invention, as defined by claim 21, teaches a capacitor having a dielectric comprising tantalum nitride. In other words, the present invention, as defined by claim 21, teaches a capacitor utilizing tantalum nitride in an unconventional mode, i.e. as a dielectric.

In contrast, DeBoer does not teach, disclose, or suggest a capacitor comprising a tantalum nitride dielectric, i.e. a dielectric made from tantalum nitride. DeBoer is directed to a capacitor utilizing tantalum pentoxide as a dielectric. DeBoer specifically discloses first tantalum-comprising layer 38 preferably comprising  $Ta_2O_5$ , i.e. tantalum pentoxide. See, for example, DeBoer, column 3, lines 62-64. DeBoer further discloses second tantalum-comprising layer 40 formed over first tantalum-comprising layer 38. Second tantalum-comprising layer 40 is a barrier layer preferably comprising tantalum and nitrogen. See, for example, DeBoer, column 4, lines 7-8. Thus, in DeBoer, tantalum and nitrogen are utilized to form a metallic barrier layer, i.e. second tantalum-comprising layer 40, and not a ceramic dielectric layer. Use of metallic tantalum nitride as a barrier layer or otherwise is well known in the art.

Moreover, DeBoer discloses a metal nitride layer, i.e. layer 42, formed over second tantalum-comprising layer 40. See, for example, DeBoer, column 4, lines 65-66. In DeBoer, metal nitride layer 42 can be formed by a conventional CVD process. Thus, in DeBoer, second tantalum-comprising layer 40 prevents carbon present from the CVD process from diffusing into first tantalum-comprising layer 38. See, for example, DeBoer, column 5, lines 3-9. Thus, DeBoer teaches a metallic barrier layer comprising tantalum and nitrogen, i.e. second tantalum-comprising layer 40, protecting a dielectric made from tantalum pentoxide, i.e. first tantalum-comprising layer 38, from carbon diffusion resulting from the formation of metal nitride layer 42 by a CVD process. For the foregoing reasons, Applicant respectfully submits that the present invention defined by independent claim 21 is not suggested, disclosed, or taught by DeBoer.

With respect to Jain, although Jain discloses the use of a copper seed layer, Jain does not suggest, disclose, or teach a tantalum nitride dielectric. Thus, for the foregoing reasons, Applicant respectfully submits that the present invention as defined by independent 21 is not suggested, disclosed, or taught by DeBoer, either singly, or in combination with Jain.

The present invention, as defined by independent claim 34, teaches a capacitor comprising a bottom interconnect metal segment, a first barrier layer, a seed layer, a dielectric, a second barrier layer, and a top interconnect metal segment all fabricated in a single tool. As disclosed in the present application, due to the novel fabrication and use of the inventions' ceramic tantalum nitride as a capacitor dielectric, the invention's

capacitor can be advantageously fabricated in a single IMP tool without having to remove the semiconductor wafer from the IMP tool for fabrication of the dielectric layer. See, for example, page 13, lines 5-9 in the present application. In other words, the invention's capacitor can be fabricated without breaking the vacuum by removing the semiconductor wafer from the IMP tool to fabricate the dielectric layer. Thus, by not breaking the vacuum and fabricating all the different layers of the invention's capacitor using the same IMP tool, a higher throughput and a higher degree of automation can be achieved in the fabrication of the invention's capacitor. Moreover, by fabricating the invention's capacitor in a single tool without breaking the vacuum, the risk of contaminating the semiconductor wafer is reduced, resulting in an advantage of a lower defect density.

In contrast, DeBoer does not teach, disclose, or suggest a capacitor comprising a bottom interconnect metal segment, a first barrier layer, a seed layer, a dielectric, a second barrier layer, and a top interconnect metal segment all fabricated in a single tool. DeBoer specifically discloses preferably forming second tantalum-comprising layer 40 by exposing an outer surface of first tantalum-comprising layer 38, i.e. a dielectric layer, to a nitrogen-comprising ambient utilizing a plasma to generate an active nitrogen species. See, for example, DeBoer, column 4, lines 6-29. DeBoer further discloses forming metal nitride layer 42 by a CVD process. See, for example, DeBoer, column 5, lines 3-6. Additionally, DeBoer states that first capacitor plate 34, preferably comprising conductively doped polysilicon, can be formed by conventional methods. See, for example, DeBoer, column 3, lines 54-59. However, DeBoer does not disclose a single

tool for fabricating a capacitor comprising a bottom interconnect metal segment, a first barrier layer, a seed layer, a dielectric, a second barrier layer, and a top interconnect metal segment. For the foregoing reasons, Applicant respectfully submits that the present invention defined by independent claim 34 is not suggested, disclosed, or taught by DeBoer.

With respect to Jain, although Jain discloses the use of a copper seed layer, Jain does not suggest, disclose, or teach a capacitor comprising a bottom interconnect metal segment, a first barrier layer, a seed layer, a dielectric, a second barrier layer, and a top interconnect metal segment all fabricated in a single tool. Thus, for the foregoing reasons, Applicant respectfully submits that the present invention as defined by independent 34 is not suggested, disclosed, or taught by DeBoer, either singly, or in combination with Jain.

The Examiner has further rejected dependent claims 8 and 9 under 35 USC 103(a) as being unpatentable over Saia in view of U.S. patent number 5,170,318 to Catala et al (“Catala”). As discussed above, independent claim 7 is patentably distinguishable over Saia and, as such, dependent claims 8 and 9 are, a fortiori, also patentably distinguishable over Saia. Moreover, the features of independent claim 7, for example a dielectric comprising ceramic tantalum nitride situated between a first and second capacitor electrode, are not suggested, disclosed, or taught anywhere in Catala. As such, independent claim 7 as well as claims 8 and 9 depending therefrom are also patentably distinguishable over Saia in combination with Catala.

Based on the foregoing reasons, the present invention, as defined by independent claims 7, 21, and 34, and claims depending therefrom, is patentably distinguishable over the art cited by the Examiner. Thus, claims 7-11 and claims 21-47 pending in the present application are patentably distinguishable over the art cited by the Examiner. For all the foregoing reasons, an early allowance and issuance of claims 7-11 and claims 21-47 pending in the present application is respectfully requested.

Respectfully Submitted,  
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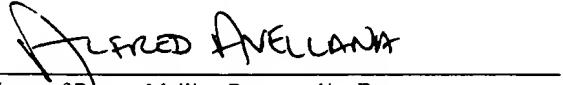
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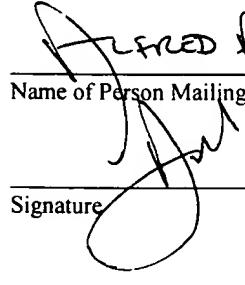
  
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